

**ANALYZE PLLs, SWITCHED-CAPACITOR FILTERS, AND OTHER CIRCUITS WITH THIS SIMULATION METHOD, WHICH YIELDS REGULAR LOOP MEASUREMENTS, SUCH AS GAIN AND PHASE MARGINS, DIRECTLY FROM THE TRANSIENT SIMULATION OF THE ORIGINAL DISCONTINUOUS SYSTEM.**

# Solving the loop-analysis puzzle

**L**OOP ANALYSIS OF ANALOG and mixed-signal discontinuous systems, such as PLLs, delta-sigma converters, switched-capacitor filters, PWM amplifiers, and switch-mode power supplies, presents a unique problem. The conventional method relies on ac analysis of a network of linear models that mimic the low-frequency behavior of each loop component. But the linear models don't reflect the underlying circuits of the original components. How do you know that the models are correct and that the results are meaningful?

## WHAT IS LOOP ANALYSIS?

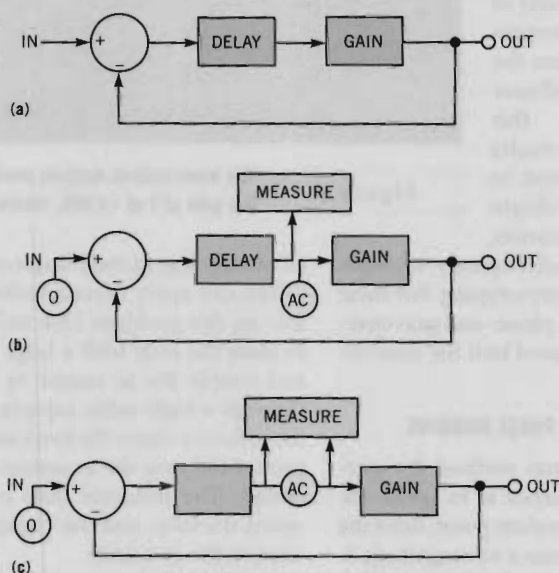
You often use negative feedback to control the output of a process. Examples range from temperature and flow control in oil refineries to simple operational amplifiers. You use negative-feedback circuits to linearize somewhat-nonlinear gain devices, such as audio amplifiers; to allow a small signal to control a large process; to provide a method of multiplying frequencies, such as in a PLL; and for many other applications. **Figure 1a** shows the classic control loop.

In an ideal world, you would never need to worry about loop analysis. Unfortunately, you cannot achieve gain alone; all components cause delay, which can cause the ideal control loop—pure negative feedback—to become significantly less than ideal—pure positive feedback. The most common technique to compensate for this problem is to add a lowpass filter in the forward path to reduce the loop gain for higher frequency signal components before the parasitic delays can drive the loop phase to  $360^\circ$ .

Unfortunately, lowpass filters themselves add  $90^\circ$  of phase shift. So, even if no other parasitic delays exist, the total loop-phase shift is  $270^\circ$ , leaving only  $90^\circ$  before the loop becomes unstable. And, in practical terms, it only takes  $30$  to  $45^\circ$  of parasitic shift for the control loop to begin to exhibit unacceptable behavior. Phase- and gain-margin analyses allow proper analysis and compensation for this shift.

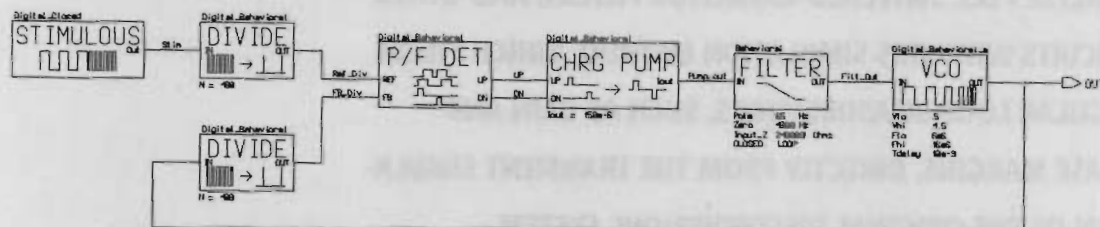
Phase- and gain-margin analysis is a common and reliable method for predicting control-loop be-

**Figure 1**



In a negative feedback loop (a), a fixed delay represents greater phase shift for higher frequency components; when total phase shift is  $360^\circ$ , feedback is positive, and the loop may be unstable. The phase margin is  $360^\circ$  minus the total loop phase shift when loop gain is equal to 1. You can measure phase and gain margin simply by breaking the loop (b), inserting a stimulus, and making direct ac measurements. You get only ac figures, however, and you cannot carry out this analysis if the loop has high dc gain. A better way to drive the loop uses a series stimulus with zero dc and fixed ac drive levels (c); the loop reaches a steady-state dc condition.

Figure 2



Build the simulation model of the PLL using standard library models or blocks of HDL-A code.

havior over a wide operating range. By examining the gain and phase within the bandwidth of the control loop, you can accurately predict the closed-loop performance of the design. Likewise, by examining the gain and phase at the limit and outside the loop's bandwidth, you can accurately predict the stability of the loop.

You can extend these techniques to a family of gain- and phase-margin analyses to examine the behavior of nonlinear systems. Also, this method produces results in a similar format to those you can obtain from test instruments, such as network and frequency-response analyzers, during prototyping. For these and other reasons, phase- and gain-margin analysis is a good tool for control-loop design.

### MEASURE GAIN AND PHASE MARGINS

The conventional method for performing loop analysis is to break the loop at some convenient point, drive the loop with an ac source of magnitude 1, and perform a standard ac analysis (Figure 1b).

However, this method works only in low-gain or perfectly ideal systems in which the loop can reliably be biased into its linear region. If any of your models include dc offsets (such as input-offset voltage) and saturation limits (such as the finite output voltage), it is nearly impossible to bias your circuit such that

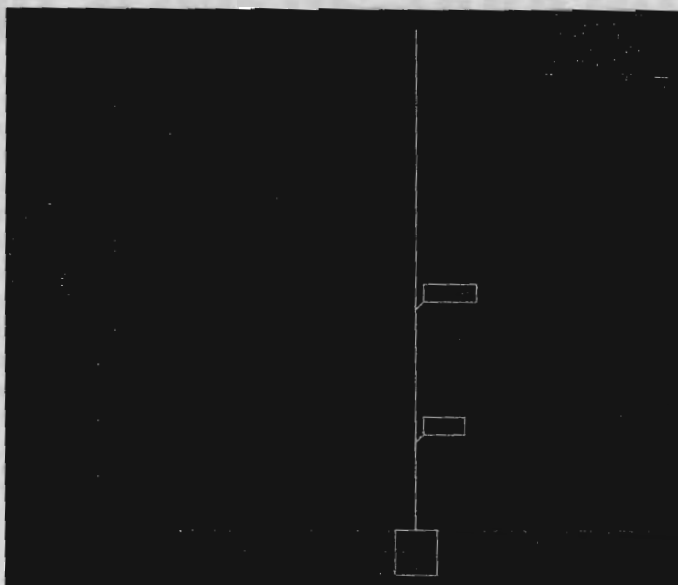


Figure 3

The open-loop-ac analysis result shows that the loop has gain of 1 at 1.6 kHz, where the phase margin is 24°.

all models stay in their linear range.

You can apply several techniques to solving this problem. One technique is to close the loop with a large inductor and couple the ac source to the loop through a high-value capacitor. At dc, the inductor closes the loop, and the capacitor removes the ac source from the circuit. The inductor then essentially opens the loop, and the capacitor connects in the ac source.

Another technique is to break the loop with an ac resistor, which is a standard component available with Mentor's Eldo analog simulator. You can set this device to exhibit extremely low resistance to dc and extremely high resistance to ac. You could also create a similar device if you are coding inHDL-A or VHDL-AMS.

However, with the freedom that the simulation environment gives you, the

most universal method for opening the loop is to place the stimulus source in series with the loop at a convenient point to break the loop (Figure 1c). You then set the stimulus with a dc magnitude of zero and an ac magnitude of any convenient value. In that way, you short the dc loop so that it can find a stable operating point, and the loop opens above zero and provides a loop perturbation.

You can then measure the gains and phases anywhere around the loop by dividing the complex ac results of the measured point by the reference point and calculating the magnitude and phase of the results (or measuring the two points, and subtracting their decibel magnitudes and phases).

To measure the entire loop, divide the signal directly upstream of the stimulus by the signal directly downstream of it.

This technique is also useful for breaking control loops that lack a low-impedance source driving a high-impedance load. Examples of this technique include a transistor amplifier, in which the base of a stage loads the collector of the previous stage.

However, all these techniques require development of reliable ac models for all the loop components. Fortunately, this task is not difficult.

### MODELING DISCONTINUOUS DEVICES

To develop a linear model, consider the behavior of the circuit without the high-frequency carrier. For instance, a PWM

forms a constant-voltage and -frequency output whose duty cycle is proportional to the input voltage. Removing the high-frequency component of the output signal yields a signal whose voltage is exactly proportional to the input voltage. So, a simple linear model for a PWM is a gain block.

If the PWM is a sampling device, then add pure delay to the model ( $e^{-j\omega \cdot \text{delay}/2\pi}$ ) that equals one sampling period. If the PWM is not a sampling device and has a triangle-generated, double-edged output, add just enough delay to represent the propagation delay of the digital portion of the circuit.

A voltage-controlled oscillator (VCO) produces a constantly increasing output phase, whose slope is directly proportional to the input voltage. So, you model a simple VCO as an integrator with gain. Again, you can add a delay of one cycle or only pure propagation delay, depending on the design of the VCO.

A frequency divider takes a constantly rising phase as an input and produces a constantly rising phase at the output. The slope of the output signal to the slope of the input signal is equal to the division ratio of the device. Therefore, a simple linear model of a frequency divider is just a constant attenuator.

A phase detector compares the values of two constantly rising input-phase signals and outputs the difference in phase. A simple linear model for this is then a subtracter. You can add cycle slipping by taking the modulus  $2\pi$  of each input before performing the subtraction. This technique is useful for linear-transient analysis, for example. Note that the exact gain of this phase-detector model depends on the output voltage of the device and on whether the device is a 2, 4, or 6 $\pi$  design.

You can easily model delay by multiplying the signal with a value of  $e^{-j\omega \cdot \text{delay}}$ . In a simple HDL-A (analog hardware-description language) model for a VCO, the primary line of interest states that the output voltage is equal to the integral of the input voltage times a constant (Listing 1). You calculate the constant using input parameters specifying the end-



**Figure 4** Plotting the closed-loop ac results shows peaking of the gain plot, corresponding to ringing in the transient response.

points of the active range of the device.

To add delay to this HDL-A model, you would add the following factor to this line:

```
Dig_OUT.v% = twopi*slope*
INTEG(a_in)*exp(0.0,1.0)*complex
(omega,0.0)*complex(delay,0.0)),
```

where "omega" is a keyword that equals the current ac analysis step, and "delay" is a constant—usually the period of the slowest expected frequency from the VCO—that a user enters.

To ensure that the models you have chosen are correct, you could check their step responses and hope for the best. However, to be sure that you correctly calculated the slope of the VCO and modeled other parameters of the design, you should more carefully analyze the

design applying discontinuous open-loop analysis.

This technique applies approximately 10 harmonically related sine-wave sources as a loop perturbation to a loop that has otherwise reached steady state. You place harmonics in and around the expected crossover frequency of the loop, which occurs when loop gain is equal to 1. You set voltages low enough that all of the models will stay in their normal operating ranges. To perform the analysis, you perform a discrete Fourier transform (DFT) at points of interest around the loop. You specify the DFT such that each component you calculate centers exactly on each of the harmonics of the perturbation signal.

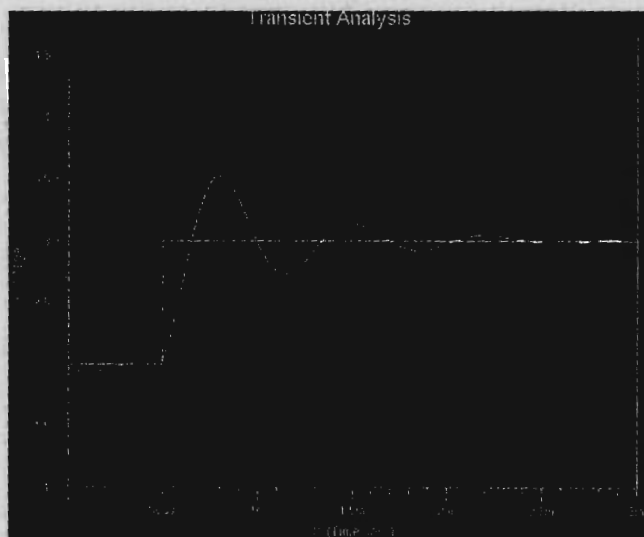
You run the simulation with all nonlinear and discontinuous models, including digital models in analog HDL, Verilog, and VHDL. In a PLL circuit, you use a model of the VCO that actually outputs digital signals. Likewise, the dividers take in a pulse stream and output a lower frequency pulse stream. As in a PLL, the signal does not re-enter the analog domain until after the charge pump enters.

You must run the simulation for at least one cycle of the lowest perturbation harmonic after the loop has reached steady state. Then, you can divide the results of the DFT for the two signals of interest while still in the complex state, or you can subtract the decibel magnitudes and phases after calculating them from the raw complex numbers.

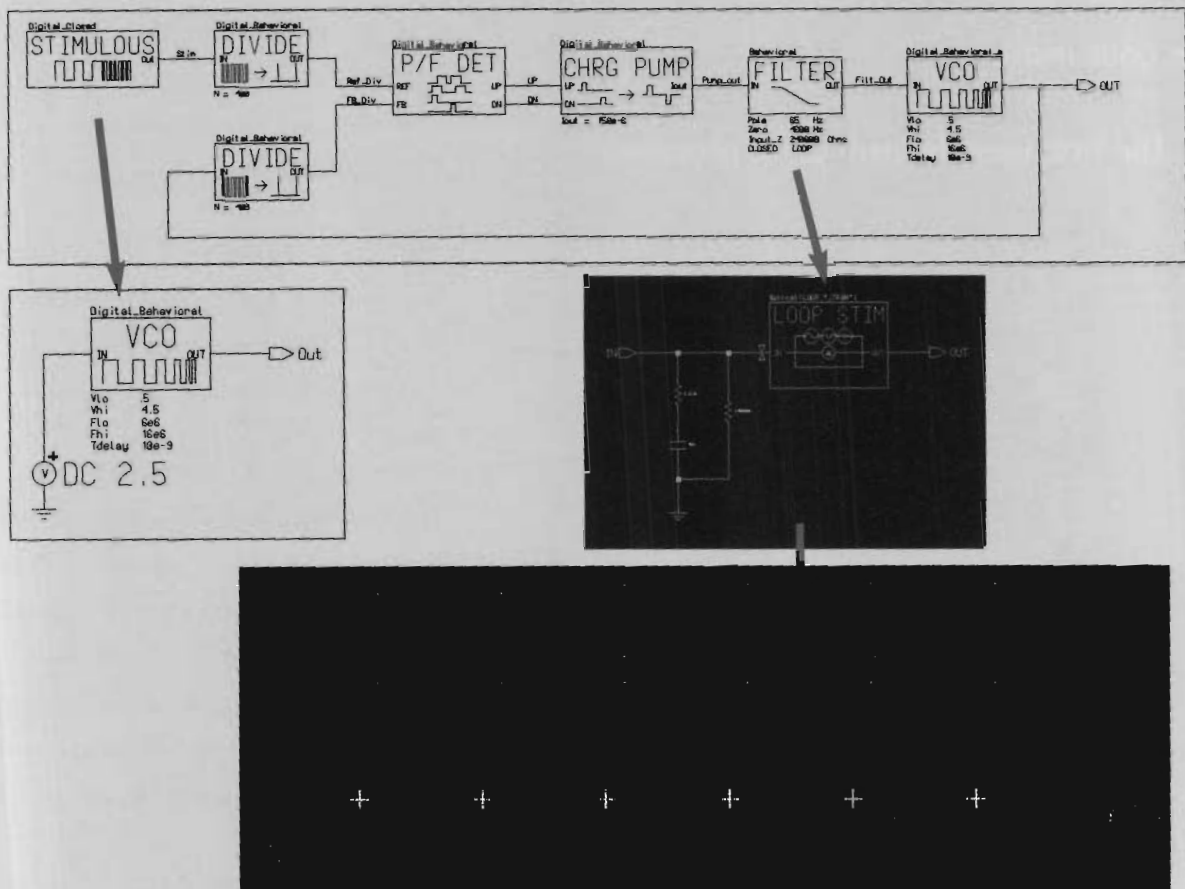
The resulting phase and gain represent the phase and gain difference between the two selected points. If you select points on either side of the perturbation source, then the results are the total gain and phase around the control loop. Then, you can perform conventional phase- and gain-margin analysis, using a phase and gain plot to determine the loop stability.

## TOP-DOWN PLL DESIGN

This example demonstrates each stage of a typical design process: building linear models; performing open- and closed-loop ac analysis, closed-loop linear-



**Figure 5** A closed-loop linear-transient plot shows ringing at the loop crossover frequency (gain=1) in response to a step input.



**Figure 6**

Configuration of the model of the PLL for the discontinuous-open-loop analysis uses a mix of library models and HDL-A coding.

transient analysis, closed-loop discontinuous-transient analysis, closed-loop IC-level transient analysis, and discontinuous open-loop analysis; and analyzing the results.

The PLL is a  $2\pi$  type, and the loop lowpass filter is a lag-lead type with a pole at 65 Hz and zero at 4 kHz (Figure 2). The limits of the VCO are 16 MHz at 4.5V and 6 MHz at 0.5V; its center frequency is 11 MHz. The dividers are a factor of 400. You model all the devices in analog HDL or with CommLib parts and perform the simulation with Accusim.

In the open-loop ac analysis, you replace the input (the stimulus block in the figure) with a short to ground. You model all components with linear models and the filter with a standard-simulation-library pole-zero function. Because these are all ideal components with no dc offsets, you can break the loop with

the conventional technique and drive it with a simple one-sided ac source.

The results show the total phase shift around the loop as being  $270^\circ$  at low frequency— $180^\circ$  from the phase detector

plus  $90^\circ$  from the VCO (Figure 3). The pole in the lead-lag filter then causes the phase to continue to shift  $90^\circ$  more toward  $360^\circ$ . The phase then reverses itself by  $90^\circ$  due to the zero in the lead-lag filter. The gain plot shows a 20-dB-per-decade slope at low frequency due to the integrator in the VCO and 40-dB-per-decade slope in the area between the pole and zero of the filter.

Measuring the phase at the frequency where the gain crosses 0 dB, you determine the phase margin to be  $24^\circ$ . The 0-dB point is where the total gain around the loop is equal to 1. This point is of interest because, below this point, the feedback cannot cause instability. If the total loop phase shift were  $360^\circ$  at the point where the total loop gain was 1, the circuit would be a stable oscillator. This loop frequen-

#### LISTING 1—HDL-A MODEL OF A VCO

```

ARCHITECTURE hdlaArchitecture_AC OF vco_ac IS
    STATE a_in : analog;
    VARIABLE slope : real;

BEGIN

    RELATION
        PROCEDURAL FOR INIT =>
            slope := (fhi_out-flo_out)/(vhi_in-vlo_in);
        PROCEDURAL FOR DC =>
            a_in := 0.0;
            DIG_OUT.v % = a_in;
        PROCEDURAL FOR AC, TRANSIENT =>
            a_in := analog_in.v;
            DIG_OUT.v % = twopi * slope * INTEG(a_in);
        END RELATION;

END ARCHITECTURE hdlaArchitecture_AC;
    
```



cy would work for a clock generator but not for a loop controlling a blast furnace!

So, in case you are thinking, "Great, so I can have negative phase margin, just as long as the phase isn't 360° when the loop gain is 0 dB," hold on! Those figures don't hold in the real world. Remember that as any component in the loop begins to exceed its operating range by clipping or saturating, the loop gain drops. Rest assured that the loop will do its best to reach the required level of saturation to reduce the gain to 0 dB where the phase crossed 360°.

The closed-loop ac analysis uses the same models as the open-loop version. The only difference is that, in closed-loop analysis, an ac source feeds the input, and a low-value resistor closes the loop. Just as you would predict, considering the 24° of phase margin, the closed-loop ac analysis shows peaking in the closed-loop gain plot (Figure 4). This peaking causes the transient response to show ringing at that frequency.

The closed-loop transient analysis again uses the same models as the open-loop version. Each HDL-A model has a procedural section that serves for both ac and transient analysis, just like the VCO model in Listing 1. You now stimulate the input with a 2.5 to 3.5V piecewise-linear (PWL) step input, closing the loop. As a result, the loop output rings at the loop-crossover frequency (Figure 5).

With linear models, this simulation runs in less than 2 sec, providing a platform for performing "what-if" testing, Monte Carlo analysis, and design centering, because you can assess the effects of many configurations and component values in a reasonable time.

#### DISCONTINUOUS OPEN-LOOP ANALYSIS

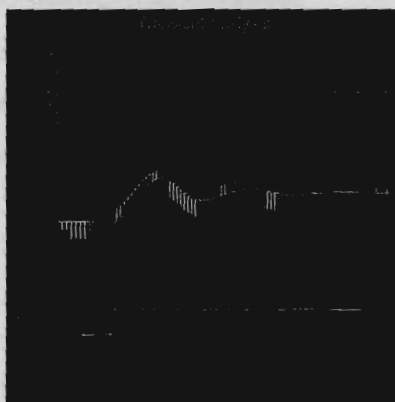
In a discontinuous open-loop analysis, the control-loop input (the "control"



**Figure 7** Raw results from the discontinuous-open-loop simulation shows the signals on each side of the series of sinusoidal sources.

value) is a fixed frequency equal to the center frequency of the VCO (Figure 6). In this case, a duplicate VCO generates this signal. You model all components with nonlinear models, discontinuous models, or both. The VCO, divider, and phase detector are all digital models built in analog HDL for mixed-mode simulation.

A series of 250- and 500-Hz and 1-, 2-, 4-, and 8-kHz sinusoidal waveforms perturb the broken loop between the filter and the VCO. The sources have a dc val-



**Figure 8** You can use linear analysis, nonlinear analysis with behavioral models, and nonlinear analysis with transistor-level models.

ue of 0V, so the loop is essentially closed for the dc analysis. The sources are pure harmonics starting at 250 Hz and ending at 8 kHz. The amplitude of the source is sufficiently small that it does not drive any loop component near the limits of its operating range. The raw results of the discontinuous-open-loop simulation show that the loop has 1 msec to settle and then is simulated for 4 msec (Figure 7). The 250-Hz term dictates the 4-msec runtime, and the 8-kHz term dictates the number of Fourier terms that must be calculated.

You could use an off-the-shelf FFT algorithm on the loop input and output signals and subtract the decibel

magnitudes and phases to obtain the loop results. But these algorithms calculate too many terms, which are spaced linearly rather than exponentially. This excess not only takes more time to compute than is necessary, but also makes the resulting chart nearly unreadable. These algorithms also have trouble handling the unevenly spaced input-data points that analog simulators typically produce.

Therefore, Mentor Graphics developed a custom Ample code DFT algorithm for this application with the following outline:

```
F(jw)=integ(exp(-jvt)*f(t))dt
using Eulers Identity:
F(jw)=integ(cos(vt)*f(t))dt -j*integ
(sin(vt)*f(t))dt
Setting A=integ(cos(vt)*f(t))dt
and B=-integ(sin(vt)*f(t))dt
then |F(jw)| = sqrt(A**2+B**2)
and phase=arctan(B/A)
```

The basic DFT algorithm is a comparison of the input signal to two orthogonal sinusoidal waves. You compare these waves by integrating the product of the sinusoid and the input signals.

The entire code listing is available with the Web-site version of this article ([www.ednmag.com/endmag.reg/2000/03162000/06ms612.htm](http://www.ednmag.com/endmag.reg/2000/03162000/06ms612.htm)). It comprises an outer loop that executes once per DFT

component with the exact frequency that corresponds to the sinusoidal waveforms in the loop perturbation. An inner loop samples the input waveforms, multiplies them by the reference sinusoids, and integrates the results. The components then turn into complex numbers from which you derive the phase and magnitude.

The results confirm that the linear models are correct; they obtain the same result of a phase margin of 24° at 1.6 kHz. When you plot the discontinuous-open-loop analysis and the linear-ac analysis on the same chart, the agreement between the two plots is to within about 1 dB over the frequency range of interest.

You can consider the use of linear-transient analysis, nonlinear-transient analysis with behavioral Models, and nonlinear-transient analysis with transistor-level models. In all three cases, you stimulate the input with a PWL step response, closing the loop. The only differences are the models that you use for each block.

The first case uses all HDL-A and

CommLib linear models. The second case is a full mixed-mode simulation using the CommLib and HDL-A nonlinear discontinuous models. The third case is a mixed-mode simulation that replaces some of the behavioral parts with an actual transistor implementation. In this case, a transistor-level implementation replaces the charge-pump model, and you model the remainder of the circuit with behavioral models. This method allows you to concentrate on one area of the design without simulating the entire design at the detail level.

The results of the three transient simulations are in reasonable agreement (Figure 8). You may notice a slight discrepancy in the transistor-level simulation. This discrepancy is caused by a design defect in the transistor-level charge pump (nonsymmetrical current pulses). This example clearly shows how well a top-down methodology reveals subtle problems that might not become known until late in the design cycle (when they are expensive to repair). As always, when you increase the level of detail in a sim-

ulation, you have to trade off simulation runtime: The behavioral simulation took 2 sec to run, the nonlinear behavioral simulation took 198 sec, and the nonlinear IC-level simulation took 628 sec. □

## AUTHOR'S BIOGRAPHY



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